REMARKS

The Office Action dated April 5, 2007 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 10 and 11 have been amended to more particularly point out and distinctly claim the subject matter which is the invention. No new matter has been added. Claims 1-6, 8-16, 18, and 19 are pending and submitted for consideration.

Claims 1-6, 10, 11, and 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,728,910 to Huang (hereinafter Huang '910). The Office Action took the position that Huang '910 teaches each element recited in the rejected claims. Applicant traverses the rejection and respectfully submits that each of claims 1-6, 10, 11, and 14-16 recite subject matter that is not taught or disclosed by Huang '910.

Claim 1, upon which claims 2-9 depend, recites a method that includes determining if a memory section is functional based on memory BIST data and selecting a redundant memory section if the memory section is determined to be nonfunctional. The method also includes determining if at least the selected redundant memory is functional according to a BIST, repeating selection of an alternate redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected. The method also

includes updating the redundant memory data structure to indicate that at least one of the selected redundant memory section or the selected alternated redundant memory section is no longer redundant.

Claim 10 recites a system including means for determining if a memory section is functional based on memory BIST data and means for selecting a redundant memory section if the memory section is determined to be nonfunctional. The system also includes means for determining if at least the selected redundant memory is functional according to a BIST, means for repeating selection of an alternate redundant memory sections, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected. The system also includes means for updating the redundant memory data structure to indicate that at least one of the selected redundant memory section or the selected alternated redundant memory section is no longer redundant.

Claim 11, upon which claims 12-16 and 18-19 depend, recites a system having a BIST capable of determining if a memory section is functional, and self-adaptive logic, communicatively coupled to the BIST, capable of selecting a redundant memory section if the memory section is determined to be nonfunctional. The BIST is further capable of determining if at least the selected redundant memory is functional, repeating selection of an alternate redundant memory section, if the selected redundant memory section or the

selected alternated redundant memory section is non-functional, until at least one of the memory is determined to be functional or all redundant memory sections have been selected and updating the redundant memory data structure to indicate that at least one of the selected redundant memory section or the selected alternated redundant memory section is no longer redundant.

Applicant submits that the cited reference of Huang '910 does not teach or suggest each of the elements recited in claims 1-6, 10, 11, and 14-16.

Huang '910 teaches a method for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory, i.e., both redundant and accessible memory portions, as a single array, preferably using a checkerboard bit pattern. In a first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During a second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored.

As noted above, Applicant submits that Huang '910 does not teach or suggest each element of the presently pending claims. Each of the presently pending claims recites, in part, repeating selection of an alternate redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected

alternated redundant memory section is determined to be functional or all redundant memory sections have been selected. Huang '910 does not teach or suggest at least these features.

Rather, Huang '910 uses the BIST test to determine bad memory locations from a memory block and then "associates" or "pairs" a good memory location in a redundant memory with the determined bad memory location from the memory block via a repair table. Once the association between the bad memory and the good redundant memory is finished, then the BIST re-tests the memory, and skips the bad memory locations during the test and instead tests the associated redundant memory locations in their place, as specified in the repair table. However, nowhere in the testing process described in Huang '910 is there any teaching or discussion of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected.

In the "Response to Arguments" section, the Office Action alleged that the selected redundant memory is the memory that is subject to testing such that the faulty rows are failed over to good redundant rows. Col. 9, lines 5-15 of Huang '910 discloses that when the BIST retests the first m rows of memory, it is actually testing a combination of accessible and redundant rows that tested good in the first stage and if an

error occurs in the first m rows during the second stage, the memory is considered non-repairable. Also see Col. 9, line 52 – Col. 10, line 9 of Huang '910.

Thus, Applicant submits that Huang '910 discloses that the testing process is only being performed twice. So, according to Huang, one BIST test is conducted to determine bad memory locations, and then after the repair table and associations are created, a second BIST test is conducted to make sure that the associations function properly. If the second BIST test fails, the method of Huang '910, as disclosed in Col. 8, lines 40-45 and Col. 9, line 52 – Col. 10, line 9, quits and determines that the memory is faulty and not useable. On the other hand, according to the present invention as disclosed in paragraph 0024-0029 of applicant's specification and recited in the presently pending claims, after the failed memory is replaced by a redundant memory, a second test is performed to check the redundant memory. If the redundant memory is also faulty, alternative redundant memory sections may be selected until the SRAM is determined to be functional or until all redundant memory sections have been tested. Therefore, after selection of alternative redundant memory sections, further tests are performed to determine if those memory sections are acceptable. In order to track which memory sections are currently redundant, the present invention, as recited in the present pending claims, updates the redundant memory data structure to indicate that a selected redundant memory section or selected alternate redundant memory section is no longer redundant.

Contrary to the present invention, there is no need for the testing method of Huang '910 to update a redundant memory structure to indicate that a block of the redundant

memory (the block used to cover for the bad memory block location) is no longer available, as there is no third or additional testing and association step that would require further association of an available redundant memory location with a bad memory location. Given the disclosure of Huang '910, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) should be withdrawn because Huang '910 does not teach or suggest each feature of claims 1, 10 and 11 and hence, dependent claims 2-6 and 14-16 thereon.

Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Publication No. 20020136066 to Huang (hereinafter Huang '066). The Office Action took the position that Huang '910 teaches each and every element recited in claim 12, except for the self adaptive logic limitations. Therefore, the Office Action combined Huang '910 and Huang '066 to yield all of the elements of claim 12. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 12.

Huang '910 is discussed above. Huang '066 teaches a system and method for a self-repairing memory that can be integrated with any BIST mechanism, without extensive modification to either the BIST or BISR mechanisms. A BISR "Wrapper" system interfaces the BIST engine to the BISR repair circuitry. The BISR Wrapper makes use of standard status signals present in any BIST engine, and directs the operation of the BISR circuitry. With the Wrapper, BISR operation need no longer be closely

coupled to the operation or internal structure of the BIST. Consequently, modification of the BIST mechanism, e.g., to improve fault coverage, can be implemented without influencing the BISR.

However, Huang '066 does cure any of the deficiencies of Huang '910, as noted above. Specifically, Huang '066 does not teach or suggest a BIST that is capable of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected, as recited in claim 11, upon which claim 12 depends. Therefore, Applicant asserts that the rejection under 35 U.S.C. 103(a) should be withdrawn because neither Huang '910 nor Huang '066, whether taken singly or combined, teaches or suggests the combination of elements recited in claim 11, and hence dependent claim 12 thereon.

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Patent No. 6,993,696 to Tanizaki (hereinafter Tanizaki). The Office Action took the position that Huang '910 teaches each and every element recited in claim 13, except for the state of a pin. However, the Office Action combined Huang '910 with Tanizaki to yield all of the elements of claim 13. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in

combination, fails to teach, show, or suggest each and every limitation recited in claim 13.

Huang '910 is discussed above. Tanizaki teaches a semiconductor memory device with a built-in self test circuit includes a semiconductor substrate, a memory cell array formed on the semiconductor substrate, an input buffer provided on the semiconductor substrate to receive externally applied data, a test circuit coupled to the memory cell array and the input buffer on the semiconductor substrate to store a program received through the input buffer to generate test data of the memory cell array according to the stored program to carry out testing of the memory cell array, and a select circuit selectively applying to the memory cell array test data applied from the test circuit and data applied from the input buffer depending upon a test operation and a normal operation.

However, Tanizaki does cure any of the deficiencies of Huang '910, as noted above. Specifically, Tanizaki does not teach or suggest a BIST that is capable of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected, as recited in claim 11, upon which claim 13 depends. Therefore, Applicant asserts that the rejection under 35 U.S.C. 103(a) should be withdrawn because neither Huang '910 nor Tanizaki, whether taken singly or combined,

teaches or suggests the combination of elements recited in claim 11, and hence dependent claim 13 thereon.

Claims 8 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Patent No. 6,181,614 to Aipperspach (hereinafter Aipperspach). The Office Action took the position that Huang '910 teaches each and every element recited in claims 8 and 18, except for where the method of performed during the manufacturing process. However, the Office Action combined Huang and Aipperspach to yield all of the elements of claims 8 and 18. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 8 and 18.

Huang '910 is discussed above. Aipperspach teaches a circuit arrangement and method of dynamically repairing a redundant memory array utilize dynamically-determined repair information, generated from a memory test performed on the redundant memory array, along with persistently-stored repair information to repair the redundant memory array. In one implementation, the persistent repair information is generated during manufacture to repair manufacturing defects in the array, with the dynamic repair information generated during a power-on reset of the array to address any additional faults arising after initial manufacture and repair of the array. Furthermore, repair of dynamically-determined errors may utilize otherwise unused redundant memory cells in a

redundant memory array, thus minimizing the additional circuitry required to implement dynamic repair functionality with an array.

However, Aipperspach does cure any of the deficiencies of Huang '910, as noted above. Specifically, Aipperspach does not teach or suggest a BIST that is capable of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected, as recited in claims 1 and 11, upon which claims 8 and 18 depend. Therefore, Applicant asserts that the rejection under 35 U.S.C. 103(a) should be withdrawn because neither Huang '910 nor Aipperspach, whether taken singly or combined, teaches or suggests the combination of elements recited in claims 1 and 11, and hence dependent claims 8 and 18 thereon.

Claims 9 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S. Publication No. 20030014619 to Cheston (hereinafter Cheston). The Office Action took the position that Huang'910 teaches each and every element recited in claims 8 and 18, except for where the method is performed during circuit power up. However, the Office Action combined Huang '910 with Cheston to yield all of the elements of claims 9 and 19. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in

combination, fails to teach, show, or suggest each and every limitation recited in claims 9 and 19.

Huang '910 is discussed above. Cheston teaches a method and system for recovering a master boot record within a data processing system. In the method, a master boot record recovery setup utility is invoked by a user. In response to invoking the master boot record recovery utility, the master boot record in a first bootable device is copied to an alternate non-volatile storage device. A recovery flag is set within BIOS indicating that the MBR has been securely copied. In response to a failed boot attempted from the first boot device, the copy of said master boot record within said alternate non-volatile storage device is accessed and utilized to boot the system.

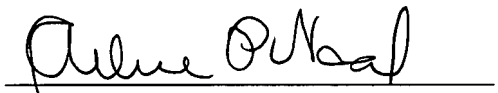
However, Cheston does cure any of the deficiencies of Huang '910, as noted above. Specifically, Cheston does not teach or suggest a BIST that is capable of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected, as recited in claims 1 and 11, upon which claims 9 and 19 depend. Therefore, Applicant asserts that the rejection under 35 U.S.C. 103(a) should be withdrawn because neither Huang '910 nor Cheston, whether taken singly or combined, teaches or suggests the combination of elements recited in claims 1 and 11, and hence dependent claims 9 and 19 thereon.

Accordingly, Applicants respectfully submit that claims 1-6, 8-16, and 18-19 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 1-6, 8-16, and 18-19 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

APN:ksh